Both the automotive industry as well as the semiconductor industry are confronted with major transformations. From the automotive perspective, more technologies and applications are needed to realize intelligent functions, optimize vehicle performance, control and decision making for future electric, connected, autonomous and shared (ECAS) vehicles mobility scenarios at affordable costs. Automotive embedded systems are highly heterogenous and contain processors that scale from 8-bit microcontrollers in legacy Embedded Control Units (ECU) all the way to high performance Central Processing Units (CPU) in autonomous driving applications. Because of the future needs of ECAS, there is a strong requirement towards new developments in terms of processor architectures, which are evolving more and more toward higher performances, while maintaining automotive requirements and very low power dissipation. These processors will be integrated in a networked mix of ECUs, domain controllers, gateways and high-performance computers (HPCs), performing several tasks, complemented by digital twins and augmented by specialized artificial intelligence processing units. In this context, the automotive industry is increasingly following the Software Defined Vehicle (SDV) paradigm, which is composed of the following main elements:

- **SDV Hardware Layer**: new low power, highly secure, high-performance system, based on a flexible and open integration of IP cores, such as mid-to-high performance processors, microcontrollers, and peripheral IP cores.
- **SDV Operating System Layer**: often called Car OS, it plays a key role in the SDV, as the intermediary layer abstracting hardware, facilitating integration, and decoupling hardware from software through a specific SDV Hardware Abstraction Layer (HAL).
- **SDV Middleware Layer**: the Car OS is further extended by a Service Oriented Framework (SOF), a middleware with an open and modular service oriented architecture, which abstracts the low-level technical details of the entire technology stack up to the vehicle OS.
- **SDV Application Layer**: this layer consists of modular building blocks and APIs which offer the functionality visible to the end-users.
This focus topic concerns an open source RISC-V based hardware system implementation of the SDV Hardware Layer compatible with one or multiple widely-agreed-upon Hardware Abstraction Layer of the vehicle of the future.

**Why open source hardware?** From the semiconductor perspective, the automotive industry is still the fastest growing market, especially for European semiconductor companies. In order to remain competitive throughout the value chain, open source is strategic for providing Europe with an alternative to licensing IPs from non-EU third parties, thereby maintaining sovereignty in the long term. A key success criterion for this is for Europe to develop a fully blown open source ecosystem so that a European fork is possible (i.e., create a fully equivalent variant of a given technology), if necessary. The realization of such an ecosystem requires a radical change in working across the board with leadership and contribution from major European industrial and research players and other stakeholders in respective application value chain actors.

**Why RISC-V?** RISC-V, being an open and extensible Instruction Set Architecture (ISA), has gained a large momentum in a number of application markets. Custom extensions can be used to improve the performance per area and power in specific applications. Such extensions are expected to be key differentiators and create a competitive area among IP and semiconductor vendors that will ensure continuous innovation of the ISA. However, RISC-V still requires important extensions and add-ons in order to support high-performance automotive quality processing needs. To close this gap and facilitate the development of top-level automotive RISC-V processor cores, efforts should be focussed on the development of an automotive RISC-V reference hardware platform, subject of this focus topic.

The expected RISC-V reference platform shall be targeted for commercial use and should comply with industry standards with respect to quality and safety. It should contain all assets and collaterals needed to enable and accelerate the development and adoption of RISC-V cores throughout the European automotive ecosystem.

In the context of the SDV paradigm, the proposed automotive RISC-V reference platform shall be considered as a specific pilot implementation of a prospective more general open and modular European reference hardware platform for the vehicle of the future. Thereby, it is very important that generic abstract SDV requirements can be mapped to the proposed RISC-V hardware architectures in order to enable complete and efficient system solutions. This is only possible in close cooperation between HW and SW developments, standardized interfaces and API’s, which need to be agreed upon.

Since the software layers of the SDV are not within scope of this focus topic, the necessary link between the RISC-V hardware developers and any SDV software development team shall be realised via a HAL, determined largely outside the proposed action. Therefore, proposers should demonstrate convincing links and collaboration plans with other European actions or communities that can provide a widely-agreed-upon industry-grade HAL description to be used as a reference for the RISC-V hardware designs in the
This focus topic addresses the hardware development part of an overall system approach for HW-SW co-design, more in particular RISC-V based processor solutions which are optimized for SDV implementations. Selected actions will be implemented as ‘linked actions’ with other EU-supported actions under ‘SDV’ and ‘RISC-V’ related topics in past calls, this call and future calls by (but not limited to) KDT JU and Chips JU. Examples of other relevant European partnerships are CCAM and 2ZERO. The notion of “linked actions” may as well be extended to nationally supported actions across the EU member states and associated states. Particular linked actions shall be clearly identified and justified in the proposals. Selected actions shall establish collaboration agreements with other relevant on-going projects and future projects. These collaboration agreements shall set out requirements for IP sharing, a common governance model, and conformity with specifications set by suitable industry bodies. Respective options under Article 3 and Article 7 of the Model Grant Agreement shall be used to this end.

Expected Outcomes

Proposal results are expected to contribute to a high-performance automotive RISC-V reference hardware platform, covering the following essential elements:

- **Instruction Set and Profile Definition:** To address the specific needs of automotive workloads and non-functional requirements (e.g. safety & security), custom instruction set extensions and profiles shall be defined. These will improve the performance of critical hot spots in applications and provide industry leading capabilities in terms of low-latency interrupts and virtualization. A special scenario of a custom multi-party extension and profile is one that subsets an existing standard extension to tailor it to automotive needs and reduce the implementation cost. Furthermore, planning differentiating features in truly innovative areas is encouraged. The development of custom single supplier extensions could be proprietary to an individual party, but still needs interaction and conformity with the rest of the reference platform. For example, related tools and solutions should be extendible with these custom extensions. At the same time, it is the expectation of customers of RISC-V solutions to receive a consistent support package including the vendor extensions.

- **Standardized Extension Interfaces:** Standardized instruction set extension interfaces greatly improve the overall offering of RISC-V cores by facilitating the design and interoperability between cores and accelerators. Ideally, the extension interface should follow an existing definition. Examples of co-processor interfaces include ARM®’s Custom Datapath Extension (CDE), CV-X-IF (maintained by the OpenHW Group), and SCAIE-V. All mentioned interfaces can interface to general-purpose accelerators. Special purpose extension interfaces can provide a more efficient interfacing, but should be limited to few key accelerators.
• **Compliance Reference Model and Validation Suite:** An *accurate reference model* capturing all platform requirements and *validation suites* are needed. The level of accuracy of the reference model depends on the granularity and level of detail of the requirements. A pragmatic trade-off should be found that allows implementers to make their own design choices while ensuring compatibility of applications with any platform. For critical parts of an operation, such as interrupts and context switching, the accuracy is assumed to be close to cycle accurate. In addition to the model itself, a *validation suite* should be developed to enable *consistency check* between any core and the reference model. Such validation of compliance is expected to be performed on intake of IP and SoCs.

• **Benchmarks:** Benchmarks are intended to assess the automotive platform throughout all the phases of its development, which implies being able to run them in environments with varying degrees of maturity, ranging from simulation environments, to FPGA prototypes, test chips, and finally, fully-fledged silicon products. Therefore, the span of environments requires *incremental benchmarking* covering different levels of abstraction. Diverse workloads shall be built and run combining items of potentially different levels, running concurrently – serialized and in parallel – mimicking relevant automotive workloads.

• **Operational hardware prototypes:** at the end of the action, the proposals shall foresee operational hardware prototypes to justify the targeted TRL 4-6. These hardware prototypes may incorporate off-the-shelf components, reconfigurable hardware, as well as engineering silicon, designed and produced as part of the proposed action. The prototypes shall demonstrate the claimed advanced high-performance features of the developed automotive RISC-V hardware designs and their conformity with the HAL. Furthermore, efficient implementations of a set of SDV software specifications shall be also demonstrated.

• **Software and Tools:** An ecosystem of software and tools is essential for the adoption of a HW platform. Domain-specific requirements like safety-qualification and the additional ISA extensions necessitate work on software and tools that goes beyond ongoing open-source community efforts. All deliverables should be extensible by third parties to facilitate the integration of vendor-specific extensions. An instruction accurate model is needed for software development in virtual prototypes. The long development cycles for SoC based on modern silicon technologies and the focus by OEMs on SW platforms requires early development enablement. The instruction accurate model is expected to execute orders of magnitude faster than the compliance model. After start of production (SOP), it can be used in digital twins, supporting the vision of the software defined vehicle.

**Scope**

In automotive industry, being no exception from general CPS development trends, SW requirements and HW implementations change over time, which poses a need for an automated process to continuously evaluate different HW SoCs under changing SW requirements. The SDV paradigm provides an efficient mechanism to decouple HW from
SW development while preserving system’s integrity and ensuring the propagation of functional and non-functional specifications across system’s abstraction layers. The key role for this decoupling of design concerns is attributed to the HAL in the SDV abstraction model. This focus topic assumes a collaborative agreement with representative European stakeholders on a reference HAL and targets an efficient hardware implementation of the latter based on RISC-V. Proposals need to particularly address but are not limited to the following hardware design aspects:

- Sound tool-agnostic collaboration infrastructure based on joint APIs for automating the continuous assessment process and DSLs for iterating over different HW configurations. This infrastructure promotes and enables new flexible RISC-V based solutions for existing and new use-cases. The planned infrastructure will allow fast and seamless comparison to existing solutions in the different design phases.
- Open high-performance RISC-V based automotive processor reference architecture, which can lead to customized instantiations towards specific automotive needs and control domains, including e.g. a superscalar architecture. It should also include a fast context switch with multi-threading support and fast deterministic interrupt/execution response.
- Integrated vector unit(s) including custom extensions as e.g. DSP, AI, networking, etc. These should be scalable with chained registers and out-of-order execution.
- Co-processor interface for special VPU and accelerators
- Safety and security elements, extended to memory and interconnect. This should include spatial and temporal redundancy for temporary and permanent faults and ASIL certification. Security features should include secure enclave and potentially execution guard. Focus should also be on micro-architectural protection for side-channel attacks and SESIP certifications.
- Exploration of different on-chip and off-chip interconnect solutions based on existing SotA (e.g. AMBA) or new developments (e.g. chiplets)
- Virtualization support with Hypervisor.
- Definition and adoption of standardised data formats, interfaces (APIs) and improved interoperability.
- Mechanisms to capture and manage, from the software level, functional as well as non-functional characteristics of possible integration with SDV modules with particular focus on real-time operation, low power dissipation, handling of (precise) computational exceptions and interrupts.
- Benchmarks and workloads for incremental hardware development. These must be usable on COTS HW, FPGA prototypes, simulators as well as emulators and must be also applicable for bare-metal and to top of full SW stacks, including hypervisors and RTOS. Multiple levels of incremental evaluations should be also supported. Finally, a trade-off between representativeness of the software and confidentiality constraints must be made.
Although the development of design software and tools is not a primary subject of this focus topic, efforts and resources needed to develop software enabling or facilitating the design of any of the essential elements of the hardware platform shall be eligible for funding.

The consortium should be coordinated by a leading European industrial actor of the automotive industry value chain, or by a neutral organisation well established in the sector. The consortium must include:

- a representative number of European semiconductor companies with headquarters in several Member States;
- a representative number of European tier-1 automotive suppliers and technology companies with headquarters in several Member States;
- a representative number of European OEMs of motorised vehicles (passenger cars, trucks, buses, motor cycles) with headquarters in several Member States;
- innovative SMEs across the value chain;
- universities and research and technology organisations bringing the newest advances in relevant digital and other technologies and/or acting act as neutral mediators.

Proposals are encouraged:

- To allocate tasks to cohesion activities with the projects selected under the call HORIZON-KDT-JU-2023-3-CSA Topic 3 on Coordination of the European software-defined vehicle platform and the call HORIZON-KDT-JU-2023-2-RIA Topic 2 on Hardware abstraction layer for a European Vehicle Operating System.
- To allocate tasks to cohesion activities with the projects selected under the previous calls HORIZON-KDT-JU-2021 and -2022 (TRISTAN & ISOLDE).
- To allocate tasks to cohesion activities with the [call 2024 SDV].
- To allocate tasks to cohesion activities with the [related CCAM and 2ZERO projects].

Specific conditions
All the specific conditions (admissibility, eligibility, evaluation criteria, scoring and threshold, etc) are the same as for Topic 1 of this call except:

Reimbursement rate for establishing the EU contribution
Reimbursement rates as percentages of the eligible cost according to HE.

<table>
<thead>
<tr>
<th>Type of beneficiary</th>
<th>EU Contribution as % of the Eligible Cost according to HE (*)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Large enterprise (for profit organization but not an SME)</td>
<td>25 %</td>
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<tr>
<td>SME (for profit SME)</td>
<td>35 %</td>
</tr>
<tr>
<td>University/Other (not for profit)</td>
<td>35 %</td>
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(*) beneficiaries may ask for a lower contribution

Capping:

The EU contribution per project is capped at 20M€ and the maximum contribution per partner in a project is limited to 40% of the total EU funding for the project.

The maximum number of participants is 70.